

A Detailed view of cortical microcircuit mapping

The diagram illustrates a hierarchical neural network structure across six layers, labeled layer 1 to layer 6 on the left. A dashed blue box encloses the main processing area, labeled 'unit' at the bottom right. The layers are defined by horizontal lines: layer 1 (top), layer 2/3, layer 4, layer 5, layer 6, and layer 7 (bottom). The network includes several components: a 'PC' (Pyramidal Cell) in layer 4, a 'memory cell' in layer 5, and an 'output' node in layer 6. A 'sensory input' (orange arrow) enters from the bottom, passing through layer 6 and layer 5 to reach the 'PC' in layer 4 (labeled 1). The 'PC' in layer 4 sends an inhibitory signal (dashed line with a red circle labeled 'inh.' and a T-bar) to the 'memory cell' in layer 5 (labeled 2). The 'memory cell' in layer 5 sends an inhibitory signal (dashed line with a red circle labeled 'inh.' and a T-bar) to the 'output' node in layer 6 (labeled 4). The 'output' node in layer 6 sends a signal (dashed line) to the 'PC' in layer 4 (labeled 3). The 'PC' in layer 4 also sends a signal (dashed line) to the 'output' node in layer 6 (labeled 4). The 'output' node in layer 6 sends a signal (dashed line) to the 'PC' in layer 4 (labeled 3). The 'output' node in layer 6 sends a signal (dashed line) to the 'PC' in layer 4 (labeled 3). The 'output' node in layer 6 sends a signal (dashed line) to the 'PC' in layer 4 (labeled 3).

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